



1 TITLE OF THE INVENTION

2 **Photovoltaic Solid State Relay**

3 BACKGROUND OF THE INVENTION

4 Field of the Invention

5 The present invention relates generally to solid state relays and more
6 specifically to a photovoltaic solid state relay using a bidirectional switch.

7 Description of the Related Art

8 A photovoltaic solid state relay as disclosed in Japanese Patent No. 2,
9 522, 249 includes a photovoltaic diode array and a bidirectional switch
10 formed by a pair of MOSFETs series-connected across a pair of output
11 terminals. The diode array responds to light from a light-emitting diode to
12 generate a voltage corresponding to an electrical control signal supplied to
13 the light-emitting diode. The voltage developed across the photovoltaic
14 diode array is supplied through a discharging circuit to the transistors and
15 applied across their gate electrodes and source electrodes so that the
16 transistors are turned ON, establishing a current conducting path across a
17 pair of output terminals to which an external load circuit is connected. For
18 using the relay in an alternating current load circuit, the source-drain paths of
19 the transistors are connected in opposite sense to each other. Since the
20 impedance across the output terminals, which is desired to be as small as
21 possible, equals the sum of on-resistances of the two transistors, a need exists
22 to reduce the resistance across the output terminals. Furthermore, if the
23 bidirectional switch is used for heavy load circuits, the source and gate
24 electrodes must be connected to respective pads to provide the ability to carry
25 high load current. However, the provision of such a pad structure requires a
26 p-type well to be formed immediately below the pads. This structure would
27 cause the capacitance of the relay to significantly increase, particularly when
28 operating at high frequencies. Therefore, a need exists to reduce the
29 capacitance of a bidirectional solid state relay for high frequency operation
30 with a heavy load circuit.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a photovoltaic solid state relay having a low output impedance.

Another object of the present invention is to provide a photovoltaic solid state relay having a low capacitance.

According to the present invention, there is provided a photovoltaic solid state relay having a pair of output terminals, comprising light emitting means for emitting light in response to an electrical control signal, first and second photovoltaic devices optically coupled to the light emitting means for converting the light to first and second voltages, respectively, and first and second unipolar transistors having first and second controlling electrodes for respectively receiving the first and second voltages and jointly establishing a first current conducting path between the output terminals. A bipolar transistor is provided having a base connected to a junction between the first and second unipolar transistors for establishing a second current conducting path in parallel to the first current conducting path between the output terminals in one of opposite directions depending on voltages applied to the output terminals.

In a preferred embodiment, the first and second unipolar transistors and the bipolar transistor are fabricated on a common semiconductor-on-insulator structure comprising a semiconductor substrate, a first insulator layer on the substrate, and a semiconductor layer on the first insulator layer. First and second backgate regions are formed in the semiconductor layer and first and second source regions are respectively formed in the first and second backgate regions. A common drain/base region is formed in the semiconductor region between the first and second backgate regions. A first insulated gate electrode is provided, bridging the first source region and the common drain/base region, and a second insulated gate electrode is provided, bridging the second source region and the common drain/base region. A second insulator layer is provided on the semiconductor layer. On

1 the second semiconductor layer, first and second gate pads are formed and
2 respectively connected to the first and second insulated gate electrodes to
3 function as the first and second controlling electrodes of the unipolar
4 transistors. On the second insulator layer, a first source pad is formed and
5 connected to the first source region and the first backgate region and a second
6 source pad is formed and connected to the second source region and the
7 second backgate region, the first and second source pads being respectively
8 connected to the output terminals. With this arrangement, the common
9 drain/base region functions as a common drain of the first and second
10 unipolar transistors and as the base of the bipolar transistor, and the first and
11 second backgate regions respectively function as an emitter and a collector of
12 the bipolar transistor when the first source pad is biased at a voltage higher
13 than the second source pad, and respectively function as a collector and an
14 emitter of the bipolar transistor when the second source pad is biased at a
15 voltage higher than the first source pad.

16 For proper operation of the bipolar transistor, the first backgate region
17 and the first source region are preferably in the shape of a first loop and the
18 second backgate region and the second source region are in the shape of a
19 second loop on the outer side of the first loop. The common drain/base
20 region is in the shape of a loop between the first and second loops. The first
21 insulated gate electrode is in the shape of a loop lying on the first loop and
22 the second insulated gate electrode is in the shape of a loop lying on the
23 second loop. The semiconductor layer is formed with first and second wells
24 of conductivity type opposite to conductivity type of the semiconductor
25 layer, the first well being surrounded by the common drain/base region and
26 the common drain/base region being surrounded by the second well, the first
27 and second wells penetrating through the semiconductor layer to the first
28 insulator layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described in detail further with reference to the following drawings, in which:

Fig. 1 is a circuit diagram of a prior art photovoltaic solid state relay;

Fig. 2 is a side view of a prior art solid state bidirectional switch integrated on a single semiconductor substrate;

Fig. 3 is a circuit diagram of a photovoltaic solid state relay of the present invention, including a bidirectional switch integrated on a common silicon substrate;

Fig. 4 is a plan view of the bidirectional switch of Fig. 3;

Fig. 5 is a cross-sectional view taken along the line 5-5 of Fig. 4;

Fig. 6 is a cross-sectional view taken along the line 6-6 of Fig. 4;

Fig. 7 is a cross-sectional plan view taken along the lines 7-7 of Fig. 5, partly broken to reveal underlying layers;

Fig. 8 is a graphic representation of load voltage versus load current characteristic of the present invention; and

Fig. 9 is a circuit diagram of a modified embodiment of the present invention.

DETAILED DESCRIPTION

Before proceeding with the detailed description of the present invention, the prior art photovoltaic bidirectional solid state relay, disclosed in Japanese Patent No. 2, 522, 249, will be described with reference to Figs. 1 and 2. In the prior art solid state relay, the application of an electrical signal from an external source, not shown, across input terminals 1a and 1b causes a light-emitting diode 2 to emit light to a photovoltaic diode array 3, where the incident light is converted to an electrical signal, which is applied to a discharging circuit 5 including a thyristor 11 which is OFF at this instant. A voltage developed in the photovoltaic diode array 3 causes diodes 9 and 10 of the discharging circuit to be forward-biased, allowing that voltage to be applied across the gates of enhancement type N-channel MOSFETs 6 and 7

1 and their common source. The drains of these transistors are to output
2 terminals 8a, 8b. Because of the enhancement type, the transistors 6 and 7 are
3 normally OFF. Hence, the output terminals 8a, 8b present "normally-open
4 contacts" to a load circuit before the input voltage is applied to the terminals
5 1a, 1b. In response to the application of a voltage across the gate electrodes
6 and the common source electrode of transistors 6 and 7, these transistors are
7 turned ON, establishing a current conduction path between the output
8 terminals 8a, 8b.

9 When the externally applied voltage is removed from the input
10 terminals 1a, 1b, the voltage across the photovoltaic diode array 3 decays
11 with time due to its self-discharging action, causing the diodes 9 and 10 to be
12 turned OFF. As a result, the impedance of the negative and positive gates of
13 the thyristor 11 rises sharply, setting the thyristor in a state ready for
14 conducting. With a further voltage drop across the photovoltaic diode array
15 3, one of the gates of the thyristor 11 is forward-biased, causing it to turn ON.
16 This results in a low impedance path being established across the gates and
17 common source of the transistors 6, 7. Because of the self-holding nature of
18 the thyristor, the ON state of the thyristor persists until the potential across
19 its anode and cathode drops to 1 volt. Transistors 6, 7 discharge their stored
20 energy through the thyristor 11 and turn OFF.

21 Transistors 6 and 7 are connected in series in opposite sense to each
22 other. This anti-serial connection enables the solid-state relay to operate in a
23 bidirectional mode. For space and cost reduction, it is undesirable to
24 fabricate the transistors 6, 7 on separate semiconductor chips. In this respect,
25 Japanese Patent No. 3,222,847 discloses a bidirectional solid-state switch
26 integrated on a common silicon substrate. As shown in Fig. 2, the
27 bidirectional solid-state switch of this prior art is comprised of a pair of
28 lateral double diffused MOSFETs of SOI (Silicon On Insulator) structure
29 formed by a silicon substrate 101, an insulating layer 102, and an n (-) type
30 silicon layer 103. On the surface of n (-) silicon layer 103 are formed two n (+)

1 drain regions 104 and 105 on which drain electrodes 114 and 115 are
2 provided, respectively. Also formed in the n (-) layer 103 between the n (+)
3 drain regions 104 and 105 is a p-type well 106 that extends from the surface of
4 layer 103 down to the insulating layer 102 and divides the layer 103 into two
5 transistor regions. In the p-type well 106 are formed two p (+) source regions
6 107 and 108 which surround the rectangular drain regions 104 and 105,
7 respectively. On the p-type well 106, are formed insulated gate electrodes 112
8 and 113 which are connected together, and a common source electrode 112
9 that bridges the source regions 107 and 108. Output terminals 8a and 8b are
10 connected to the drain electrodes 114 and 115, respectively.

11 Transistors 6 and 7 are turned ON by biasing the gate electrodes 112,
12 113 positive with respect to the source electrode 117 to create a channel
13 beneath each of the insulated gate electrodes 112 and 113. With the
14 transistors being turned ON, a current conduction path is established from
15 the output terminal 8a to the output terminal 8b by biasing the former
16 positive with respect to the latter. A current conduction path is established in
17 the opposite direction by biasing the terminal 8b positive with respect to the
18 terminal 8a. The transistors are turned OFF by discharging the channels
19 through a short-circuit path established between the common gate electrodes
20 112, 113 and the source electrode 117.

21 Since the impedance across the output terminals equals a sum of the
22 on-resistances of the bidirectional transistors, there is a need to reduce this
23 impedance particularly for heavy current applications. Furthermore, if the
24 bidirectional switch is used for heavy loads, the source and gate electrodes
25 must be connected to respective pads to provide capability to carry high load
26 current. However, the provision of such a pad structure requires the p-type
27 well 106 to be formed immediately below the pads. This structure would
28 cause the capacitance of the relay to significantly increase, particularly when
29 operating at high frequencies. Therefore, a need exists to reduce the
30 capacitance of a bidirectional solid state relay for high frequency operation

1 with a heavy load circuit.

2 Fig. 3 is a circuit diagram of a photovoltaic bidirectional solid state
3 relay according to a preferred embodiment of the present invention. In the
4 present invention, two photovoltaic diode arrays 3a and 3b are provided for
5 receiving light from the light-emitting diode 2 and two discharging circuits 5a
6 and 5b, each being identical to the discharging circuit 5 of Fig. 1, are
7 connected to the photovoltaic diode arrays 3a and 3b, respectively.

8 A bidirectional solid state switch 20 is connected to the discharging
9 circuits 5a and 5b. Switch 20 is comprised of enhancement type (normally
10 off), N-channel MOSFETs 21a and 21b having their source electrodes
11 connected to the output terminals 8a and 8b and their drain electrodes
12 connected together to a circuit node 15. The gate electrode of transistor 21a is
13 connected to the cathode of diode 9a and its source connected to the anode of
14 diode 10a. In the same way, the gate electrode of transistor 21b is connected
15 to the cathode of diode 9b and its source connected to the anode of diode 10b.

16 A PNP transistor 22 is provided having its base connected to the
17 circuit node 15. As described in detail later, the bipolar transistor 22 is
18 constructed so that when the output terminal 8a is biased positive with
19 respect to the output terminal 8b, the bipolar transistor 22 forms its emitter at
20 the output terminal 8a and its collector at the output terminal 8b, as indicated
21 by a solid line 16. When the output terminal 8a is biased negative with
22 respect to the output terminal 8b, the bipolar transistor 22 forms its emitter at
23 the output terminal 8b and its collector at the output terminal 8a as indicated
24 by a broken line 17.

25 In the absence of an electrical control signal across the input terminals
26 1a and 1b, the thyristors 11a and 11b of both discharging circuits are in the
27 OFF state. The application of an electrical signal to input terminals 1a and 1b
28 causes a light-emitting diode 2 to emit light to photovoltaic diode arrays 3a,
29 3b, producing a voltage across their terminals. In the discharging circuit 5a,
30 the voltage developed in the photovoltaic diode array 3a causes diodes 9a

1 and 10a to be forward-biased, biasing the gate of transistor 21a with respect
2 to its source electrode. Simultaneously, in the discharging circuit 5b, the
3 voltage developed in the photovoltaic diode array 3b causes diodes 9b and
4 10b to be forward-biased, biasing the gate of transistor 21b with respect to its
5 source electrode. In this manner, the transistors 21a and 21b are both turned
6 ON.

7 When the electrical control signal is removed from the input terminals
8 1a, 1b, the thyristors 11a and 11b are turned ON in the same way as described
9 in relation to Fig. 1 and energy stored on the gate electrode of each MOSFET
10 is discharged through the corresponding thyristor and both MOSFETs are
11 turned OFF.

12 Details of the bidirectional solid state switch 20 will be described
13 below with reference to Figs. 4 to 7. In the top plan view of Fig. 4, the switch
14 20 is implemented on a single semiconductor chip. Transistor 21a comprises
15 a gate pad 23a surrounded by an aluminum source pad 24a. Along the outer
16 periphery of the source pad 24a is formed a polysilicon gate electrode 39a
17 embedded in an interlayer insulator 41 in the shape of an inner race track and
18 spaced from the source pad 24a, as seen from Fig. 5. Gate pad 23a and the
19 embedded gate electrode 39a are interconnected by an embedded gate
20 polysilicon 45a as shown in Fig. 6.

21 Transistor 21b comprises a gate pad 23b surrounded by an aluminum
22 source pad 24b. Along the inner periphery of the source pad 24b is formed a
23 polysilicon gate electrode 39b embedded in the interlayer insulator 41 in the
24 shape of an outer race track so that the gate electrode 39b is isolated from the
25 source pad 24b. Gate pad 23b and the embedded gate electrode 39b are
26 interconnected by an embedded gate polysilicon 45b.

27 As illustrated in Figs. 5 and 6, the bidirectional solid state switch 20 is
28 fabricated on an SOI (Silicon On Insulator) structure 30 comprising a p-type
29 silicon substrate 31, a silicon dioxide layer 32 and an n (-) type silicon layer
30 33. Silicon substrate 31 is biased at a floating potential to reduce the drain-

1 substrate capacitance of the bidirectional switch.

2 A common n-type well 34 is formed in the n (-) silicon layer 33 in the
3 shape of a race track extending along adjacent sides of the gate electrodes 39a
4 and 39b. Within an inner area of the n (-) type silicon layer 33 that is
5 surrounded by and spaced from the n-type well 34, there is formed a p-type
6 well 44a having a depth extending to the silicon dioxide layer 32 and
7 occupying the underlying area of the source pad 24a. Along the outer
8 periphery of the p-type well 44a is formed a p-type backgate region 35a of the
9 MOSFET 21a shaped in a race track pattern, extending along the outer edges
10 of the source pad 24a, as clearly shown in Fig. 7. On the outside of the n-type
11 well 34 is a p-type well 44b having the same depth as the p-type well 44a and
12 occupying the underlying area of the source pad 24b. Along the inner
13 periphery of the p-type well 44b is formed a p-type backgate region 35b of the
14 MOSFET 21b shaped in a race track pattern surrounding the n-type well 34.
15 Therefore, the backgate region 35b extends along the inner edges of the
16 source pad 24b.

17 Along the outer periphery of the backgate region 35a is formed an n
18 (+) source region 37a of a race track pattern having a depth extending from
19 the upper surface of the backgate region 35a (Fig. 7). In the width dimension
20 (Fig. 5), the source region 37a is spaced a predetermined distance from the
21 outer edge of backgate region 35a to define a channel for the MOSFET 21a.

22 For the MOSFET 21b, an n (+) source region 37b is formed along the
23 inner periphery of the backgate region 35b with a depth extending from the
24 upper surface of the backgate region 35b. Source region 37b is spaced a
25 predetermined distance from the inner edge of backgate region 35b to define
26 the channel of the MOSFET 21b. Polysilicon gate electrode 39a and 39b are
27 insulated from the source region 37a and 38b, respectively, by gate insulators
28 38a and 38b. Between the interlayer insulator 41 and the n (-) silicon layer 33
29 is a field oxide film formed by a thick silicon dioxide layer 40.

30 As shown in Fig. 5, the n-type well 34 and the underlying portion of

1 the n (-) silicon layer 33 constitute a drain/ base region 36 which serves as the
2 common drain region of the MOSFETs 21a and 21b as well as the base region
3 of the bipolar transistor 22. Backgate regions 35a and 35b of the MOSFETs
4 21a, 21b also function as the emitter and collector regions, respectively, of the
5 bipolar transistor 22 when the source pad 24a is biased positive relative to the
6 source pad 24b, or function as the collector and emitter regions, respectively,
7 when the source pad 24b is biased positive relative to the source pad 24a.

8 Gate pads 23a and 23b are connected to the cathodes of diodes 9a and
9 9b, respectively. Source pads 24a and 24b are respectively connected to the
10 output terminals 8a and 8b to which the cathodes of diodes 10a and 10b are
11 also respectively connected.

12 When an electrical control signal is applied to the input terminals 1a
13 and 1b, the gate electrode 39a is biased positive with respect to the source pad
14 24a and the gate electrode 39b is biased positive with respect to the source
15 pad 24b, creating a channel immediately below each of the gate insulators 38a
16 and 38b. With the MOSFETs 21a and 21b being turned ON, if the source pad
17 24a is biased positive with respect to the source pad 24b, a current conduction
18 path is established between the source pads 24a and 24b through the channels
19 and the common drain/ base region 36. If the voltage between the source pad
20 24a and the common drain/ base region 36 is lower than the forward-bias
21 voltage (V_F) of 0.7 to 1.0 volt developed across the source region 37a and the
22 drain/ base region 36, the resistance between the output terminals 8a and 8b
23 is equal to the sum of on-resistances of the MOSFETs 21a and 21b. When the
24 voltage between the source pad 24a and drain/ base region 36 is higher than
25 the voltage V_F , the backgate regions 35a and 35b function as the collector and
26 emitter of the PNP transistor 22 and the transistor 22 is turned ON.

27 Therefore, in the absence of a voltage across the output terminals 8a
28 and 8b, the PNP transistor 22 is in the OFF state. When a load voltage is
29 applied across the output terminals 8a, 8b, the voltage between the source
30 pad 24a and drain/ base region 36 becomes higher than the voltage V_F . An

1 additional current conduction path is established from the backgate region
2 35a, acting as an emitter, through the base region 36 to the backgate region
3 36b, acting as a collector. In this way, the PNP transistor 22 is turned ON.

4 With the PNP transistor 22 being turned ON, the voltage across the
5 source pads 24a and 24b is equal to the saturated base-emitter voltage of the
6 transistor 22. Therefore, the resistance between the output terminals 8a and
7 8b becomes lower than the sum of the on-resistances of the MOSFETs 21a,
8 21b, i.e., lower than the total on-resistance of the prior art solid state relay of
9 Fig. 1.

10 If the output terminals 8a, 8b are biased in reverse to that described
11 above, an additional current conduction path is established in the opposite
12 direction, i.e., from the backgate region 35b through the base region 36 to the
13 backgate region 35a.

14 Bidirectional switch 20 is turned OFF when the electrical control signal
15 is removed from the input terminals 1a, 1b. When this occurs, the thyristors
16 11a and 11b are briefly turned ON, causing energy stored in the channel
17 regions of the MOSFETs 21a, 21b to be discharged. With the MOSFETs being
18 turned OFF, the bidirectional switch 20 no longer responds to a voltage which
19 may still be applied to the source pads 24a and 24b after the turn-off of the
20 transistors.

21 The voltage required to turn-on the PNP transistor 22 can be
22 determined by the gate voltages of the MOSFETs as well as by the current
23 amplification factor of the PNP transistor 22.

24 The load current versus the load voltage characteristic of the present
25 invention is shown in Fig. 8 for comparison with the prior art. For a given
26 load voltage, the present invention allows much higher load current than is
27 possible with the prior art.

28 In addition, the bidirectional solid state relay of the present invention
29 has a low capacitance compared to the prior art. As illustrated in Fig. 7, the
30 p-type wells 44a and 44b are formed below the gate pads 23a, 23b and source

1 pads 24a, 24b. These p-type wells are isolated from the overlying electrode
2 pads by means of the silicon dioxide layer 40 and the interlayer insulator 41.
3 Due to this isolating structure, the PN junction area of the bidirectional
4 switch that affects the drain-source capacitance is kept to a minimum.

5 Fig. 9 is a circuit diagram of a modification of the present invention in
6 which parts corresponding to those in Fig. 3 are marked with the same
7 numerals as those used in Fig. 3. In this embodiment, a first light-emitting
8 diode 2a is connected across a pair of input terminals 51a, 51b and a second
9 light-emitting diode 2b is connected across a pair of input terminals 51c, 51d.
10 LEDs 2a and 2b are respectively associated with the photovoltaic diode
11 arrays 3a and 3b.

12 The solid state relay of Fig. 9 operates in one of the following three
13 modes:

14 Mode 1

15 In mode 1, two electrical control signals are simultaneously applied to
16 the input terminals 51a, 51b and the input terminals 51c, 51d. In this mode,
17 the bidirectional solid state relay operates in the same manner as in the
18 previous embodiment.

19 Mode 2

20 In mode 2, only one electrical control signal is applied to one of the
21 input terminal pairs 51a to 51d so that only one of the MOSFETs 21a, 21b
22 which is connected to the output terminal whose voltage is lower than the
23 other output terminal, is turned ON. Assume that the output terminal 8a is
24 supplied with a higher load voltage than the output terminal 8b. If an
25 electrical control signal is applied across the input terminals 51c and 51d, the
26 MOSFET 21b is turned ON. When the voltage between the source pad 24a
27 and the common drain/base region 36 exceeds the voltage V_F between the
28 source region 37a and the drain/base region 36, the PNP transistor 22 is
29 turned ON. Similar event occurs if the output terminal 8b is supplied with a
30 higher load voltage than the output terminal 8a and an electrical control

1 signal is applied across the input terminals 51a and 51b. In this case, the
2 MOSFET 21a is turned ON. Since the voltage between the source pad 24b
3 and the common drain/base region 36 exceeds the voltage V_F between the
4 source region 37b and the drain/base region 36, the PNP transistor 22 is
5 turned ON.

6 Mode 3

7 In mode 3, two electrical control signals are supplied simultaneously
8 to the input terminals 51a to 51d

9 If the output terminal 8a is supplied with a higher load voltage than
10 the output terminal 8b and two electrical control signals are supplied
11 simultaneously to the input terminals 51a to 51d, the MOSFETs 21a and 21b
12 are turned ON. If the electrical signal is removed from the input terminals
13 51a and 51b before the voltage between the source pad 24a and the
14 drain/base region 36 exceeds the voltage V_F , the MOSFET 21a is turned OFF.
15 When the voltage between the source pad 24a and the drain/base region 36
16 subsequently exceeds the voltage V_F , the PNP transistor 22 is turned ON. A
17 similar event occurs if the output terminal 8b is supplied with a higher load
18 voltage than the output terminal 8a and two electrical control signals are
19 supplied simultaneously to the input terminals 51a to 51d, causing the
20 MOSFETs 21a and 21b to be turned ON. If the electrical signal is removed
21 from the input terminals 51c and 51d before the voltage between the source
22 pad 24b and the drain/base region 36 exceeds the voltage V_F , the MOSFET
23 21b is turned OFF. When the voltage between the source pad 24b and the
24 drain/base region 36 subsequently exceeds the voltage V_F , the PNP transistor
25 22 is turned ON. The solid state relay is turned OFF by clearing the electrical
26 control signal supplied to the input terminals.